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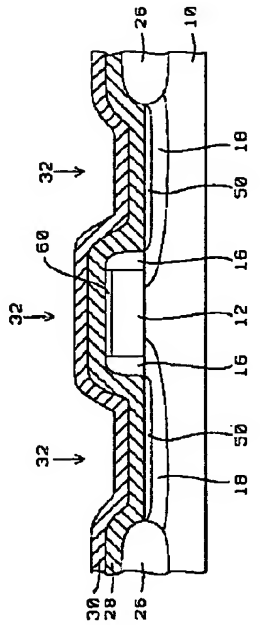
(54) **METHOD OF FORMING SILICIDE**

(57) Abstract:

PROBLEM TO BE SOLVED: To dissociate a natural oxide film when forming Ni (Pt) silicide.

SOLUTION: The method of forming silicide comprises a process of preparing a semiconductor substrate 10 provided with at least one device having exposed silicon, a process of depositing a nickel-platinum (Ni (Pt)) alloy layer 28 at least on the device, a process of depositing a titanium (Ti)-coated layer 30 on the Ni (Pt) alloy layer to form an Ni (Pt) film coated with Ti, and a process of conducting short-time annealing (RTA) 32 on the structure to form the silicide 50 on the exposed silicon.



JP2002124487A2: METHOD OF FORMING SILICIDE

CLAIMS

[Claim(s)]
[Claim 1] The formation method of silicide characterized by providing the following. The step which offers the semiconductor substrate in which at least one device which has exposed silicon was prepared. The step which makes a nickel platinum (nickel (Pt)) alloy layer deposit on the aforementioned device at least. The step which makes a titanium (Ti) enveloping layer deposit on the aforementioned nickel(Pt) alloy layer so that nickel (Pt) film which carried out Ti covering can be formed. The step which performs short-time annealing (RTA) to the aforementioned structure (substrate) so that silicide can be formed on the silicon which carried out [aforementioned] disclosure.
[Claim 2] How to be in the range whose thickness of the aforementioned nickel (Pt) alloy layer is about 50A or 300A, and be in the range whose thickness of the aforementioned Ti enveloping layer is about 30A or 300A in the method of a claim 1.
[Claim 3] How to be nickel with which the aforementioned nickel (Pt) alloy layer contains the platinum of about 0.2 atom % or 10 atom % in the method of a claim 1.
[Claim 4] The method formed when the aforementioned nickel (Pt) alloy layer carries out sputtering of the metal target material which has platinum of about 0.2 atom % or 10 atom % in nickel alloy in the method of a claim 1.
[Claim 5] The method by which the aforementioned short-time annealing is performed for 10 seconds or 60 seconds in the method of a claim 1 at the temperature of the range of about 400 degrees C or 800 degrees C.
[Claim 6] How to contain the step which makes pure the aforementioned semiconductor substrate 10 and a device for about 100 seconds or 800 seconds in front of the deposition step of the aforementioned nickel (Pt) alloy layer using HF solution of 100 to 1 in the method of a claim 1.
[Claim 7] How to contain the step which removes all nickel (Pt) alloy layer and Ti enveloping layer which remain by etchback after the aforementioned short-time annealing step in the method of a claim 1.
[Claim 8] a claim -- one -- a method -- setting -- the above -- a short time -- annealing -- a step -- after -- about -- one -- a minute -- or -- 30 -- a minute -- between -- sulfur -- a peroxide -- a mixture -- using it -- carrying out -- having -- etchback -- remaining -- all -- nickel -- (-- Pt --) -- an alloy layer -- and -- Ti -- an enveloping layer -- removing -- a step -- containing -- a method .
[Claim 9] In the method of a claim 1 after the aforementioned short-time annealing step For time about 1 minute or, and 10 minutes, By the etchback performed at the temperature of about 30 degrees C, or 70 degrees C using the mixture of the sulfur peroxide which consists of about 5% or 55% of H2SO4, about 1%, or 22.5% of H2O2 and 1%, or 22.5% of H2O The method containing the step which removes all nickel (Pt) alloy layer and Ti enveloping layer which remain.

[Claim 10] The way the aforementioned silicide consists of nickel(Pt) Si in the method of a claim 1.
[Claim 11] The formation method of silicide characterized by providing the following. The step which offers the semiconductor substrate which has at least one active region and at least one poly gate field. The step which defecates the aforementioned semiconductor substrate. The step which makes a nickel platinum (nickel (Pt)) alloy layer deposit on the aforementioned active region and the aforementioned poly gate field at least. The step which makes a titanium (Ti) enveloping layer deposit on the aforementioned nickel(Pt) alloy layer so that nickel (Pt) film which carried out Ti covering can be formed, and the step which performs short-time annealing (RTA) to the aforementioned structure (substrate) so that silicide may be formed.
[Claim 12] How to be in the range whose thickness of the aforementioned nickel (Pt) alloy layer is about 50A or 300A, and be in the range whose thickness of the aforementioned Ti enveloping layer is about 30A or 300A in the method of a claim 11.
[Claim 13] How to be nickel with which the aforementioned nickel (Pt) alloy layer contains the platinum of about 0.2 atom % or 10 atom % in the method of a claim 11.
[Claim 14] The method formed when the aforementioned nickel (Pt) alloy layer carries out sputtering of the metal target material which has platinum of about 0.2 or 10 atom % in nickel alloy in the method of a claim 11.
[Claim 15] The method by which the aforementioned short-time annealing is performed for 10 seconds or 60 seconds in the method of a claim 11 at the temperature of the range of about 400 degrees C or 800 degrees C.
[Claim 16] The method by which the step which defecates the aforementioned semiconductor substrate 10 is performed for about 100 seconds or 800 seconds in the method of a claim 11 using HF solution of 100 to 1.
[Claim 17] The method containing the step which removes all nickel (Pt) alloy layer and Ti enveloping layer which remain by etchback after the aforementioned short-time annealing step in the method of a claim 11.
[Claim 18] a claim -- 11 -- a method -- setting -- the above -- a short time -- annealing -- a step -- after -- about -- one -- a minute -- or -- 30 -- a minute -- between -- sulfur -- a peroxide -- a mixture -- using it -- carrying out -- having -- etchback -- remaining -- all -- nickel -- (-- Pt --) -- an alloy layer -- 28 -- and -- Ti -- an enveloping layer -- removing -- a step -- containing -- a method .
[Claim 19] In the method of a claim 11 after the aforementioned short-time annealing step at the temperature of about 30 degrees C, or 70 degrees C for time about 1 minute or, and 10 minutes about -- five -- % -- or -- 55 -- % -- H -- two -- SO -- four -- about -- one -- % -- or -- 22.5 -- % -- H -- two -- O -- two -- and -- one -- % -- or -- 22.5 -- % -- H -- two -- O -- from -- changing -- sulfur -- a peroxide -- a mixture -- using it -- carrying out -- having -- etchback -- remaining -- all -- nickel -- (-- Pt --) -- an alloy layer -- and -- Ti -- an
[Claim 20] The way the aforementioned silicide consists of nickel(Pt) Si in the method of a claim 11.
[Claim 21] The formation method of silicide characterized by providing the following. The step which offers the semiconductor substrate which has at least one active region and at least one poly gate field. The step which defecates the aforementioned semiconductor substrate. The step which makes nickel (Pt) alloy layer in the range whose thickness is about 50A or 300A deposit on the aforementioned active region and the aforementioned poly gate field at least. The step made to deposit on the aforementioned nickel(Pt) alloy layer so that nickel (Pt) film which carried out Ti covering of the Ti enveloping layer in the range whose thickness is about 30A or 300A can be formed, and the step which performs short-time annealing (RTA) to the aforementioned structure (substrate) so that silicide can be formed.

[Claim 22] How to be nickel with which the aforementioned nickel (Pt) alloy layer contains the platinum of about 0.2 atom % or 10 atom % in the method of a claim 21.
[Claim 23] The method formed when the aforementioned nickel (Pt) alloy layer carries out sputtering of the metal target material which has platinum of about 0.2 or 10 atom % in nickel alloy in the method of a claim 21.
[Claim 24] The method by which the aforementioned short-time annealing is performed for 10 seconds or 60 seconds in the method of a claim 21 at the temperature of the range of about 400 degrees C or 800 degrees C.
[Claim 25] The method by which the step which defecates the aforementioned semiconductor substrate 10 is performed for about 100 seconds or 800 seconds in the method of a claim 21 using HF solution of 100 to 1.
[Claim 26] The method containing the step which removes all nickel (Pt) alloy layer and Ti enveloping layer which remain by etchback after the aforementioned short-time annealing step in the method of a claim 21.
[Claim 27] a claim -- 21 -- a method -- setting -- the above -- a short time -- annealing -- a step -- after -- about -- one -- a minute -- or -- 30 -- a minute -- between -- sulfur -- a peroxide -- a mixture -- using it -- carrying out -- having -- etchback -- remaining -- all -- nickel -- (-- Pt --) -- an alloy layer -- 28 -- and -- Ti -- an enveloping layer -- 30 -- removing -- a step -- containing -- a method.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Generally this invention relates to formation of a silicide layer, and titanium covering / nickel (platinum) salicide process more specifically used for manufacture of a semiconductor device.
[0002]
[Description of the Prior Art] It is for a metal to react with silicon (Si) and to form silicide or Salicide (silicide which carried out self-adjustment) in any of whether diffusion is controlled by nucleation of the phase which grows, or to be restricted. Movement by which diffusion was controlled is observed by almost all silicide in the state where growth increases in the square root of time.
[0003] The latest titanium (Ti) or all the salicide processes of a cobalt (Co) system are reactions which restrict nucleation. Finally reduction gate length will restrict perfect phase transference of nucleation limit reaction silicide for lack of a nucleation part. This limit serves as a narrow width-of-face sheet resistance rolloff.
[0004] The method of forming a metal Salicide layer on the MOS transistor structure which lessens a possibility that the bridge of metal silicide may be formed between the source / drain field, and the poly silicon gate is indicated by U.S. Pat. No. 5,966,607 to SHI and others (Chee). It is used, in order that comparatively thin nickel or a platinum metal layer may be formed in the front face of the MOS transistor structure and may form a metal Salicide layer. Thin nickel or thin Pt metal layer in a front face of a side-attachment-wall spacer of the gate lessens possibility that the defect of metal silicide will arise.
[0005] The platinum-alloy film which performed nitrogen annealing processing is indicated by U.S. Pat. No. 6,025,205 to a park and others (Park). Specifically, on the substrate heated by 500 degrees C from the room temperature, under the atmosphere not only containing inert gas (Ar, Ne, Kr, Xe) but nitrogen, it is making Pt film deposit and

(111) or (200) (220) Pt film by which direction control was carried out is offered. Next, Pt film is annealed and the nitrogen introduced into Pt film during the manufacture is removed substantially.
[0006] The capacitor process which the first metal layer which changes from an IVB group like titanium or VB refractory-metal transition element to U.S. Pat. No. 5,668,040 to BAIUN (Byun) deposits on a silicon substrate or a silicon oxide layer is indicated. The VIII group near an abbreviation noble-metals transition element like nickel or Pt is made to deposit on the first metal layer. In order to form a high-melting point nitriding metal layer between a refractory metal and an abbreviation noble-metals layer, it heat-treats to a substrate and a metal layer in ammonia atmosphere. Moreover, if a refractory metal is made to deposit on a silicon substrate, a silicide layer will be formed between a refractory-metal layer and a substrate during heat treatment. However, if a refractory metal is made to deposit on a silicon oxide substrate, a high-melting point metallic-oxide layer will be formed during heat treatment.
[0007] The research which went to the well which investigates the influence of a natural oxide to formation of nickel silicide is indicated by the paper "the nickel-Si phase transference (On the nickel-Si Phase Transformation With/Without Native Oxide) when there is a natural oxide, / in case there is nothing" by P.S. Lee and others (Lee), by the micro electro nick engineering 51-52 (2000) and 583 - 594 pages. When he had no oxide, sputtering of the nickel film of various thickness was carried out on Si (100) wafer by the case with a natural oxide, and the case with a RTO oxide, and it was **(ed) on a RTAI nitrogen-gas-atmosphere mind for 1 minute at about 250 or 900 degrees C. It turns out that nickel film does not react below 800 degrees C, but NiSi2 is formed at 800 or 900 degrees C.
[0008] Were received at the Mat.Res.Soc.Symp.Proc. meeting of the spring of 1999. D. Formation of "(100) nickel (Pt) silicide on Si and (111) Si and stability () by the MANGE link and others (Mangelinck) [Formation and Stability of nickel(Pt) Silicide] The research result about the little influence of Pt (5at.%) to the thermal stability of the NiSi film in Si (100) and (111) Si is indicated by paper (6 pages) called on Si and (100) Si (111)." As a result of adding platinum (Pt), the nucleation temperature of a JISHIRI side (disilicide) rises to 900 degrees C, and, for this reason, the stability of NiSi in high IC temperature becomes what was further excellent.
[0009] In order to solve the thermal instability nature of nickel silicide recently, nickel platinum (nickel (Pt)) alloy silicide stable to the temperature of 900 degrees C in which the interconnection process of a back process and conformity are possible is proposed after that. However, nickel cannot return a natural oxide (SiO2) easily, but, for this reason, an interface oxide invites the serious trouble for nickel(Pt) Salicide formation. For example, if the up layer of a natural oxide (SiO2) exists on (Silicon Si) layer (natural oxide interception), nickel (nickel) will not react with Si in the time of a 500-degree C annealing temperature.
[0010]
[Problem(s) to be Solved by the Invention] Therefore, one purpose of this invention is offering the Ti cap (Ti protection) (Pt) nickel process.
[0011] Another purpose of this invention is making a natural oxide dissociate, when forming nickel (Pt) silicide. The further purpose of this invention is thermally stable, and is offering nickel system salicide process which forms nickel system silicide which is independent-like (it is not a diffusion control type but a motor type) from line breadth.
[0012] The other purposes will become clear from the following explanation.
[0013]
[Means for Solving the Problem] The above of this invention and the other purposes were understood that it can realize as follows. The semiconductor substrate in which at

least one device which specifically has silicon exposed upwards was prepared is offered. A nickel-platinum (nickel (Pt)) alloy layer is made to deposit on this device at least. A titanium (Ti) enveloping layer (protective layer) is made to deposit on nickel(Pt) alloy layer so that nickel (Pt) film which carried out Ti covering (protection) can be formed. Next, in order to form silicide on the exposed silicon, the short-time annealing (RTA) method is performed to the structure.

[0014]

[Embodiments of the Invention] The feature and the advantageous point of this invention will be understood still more clearly by reading the following explanation with the accompanying drawing which displays the element, field, and portion which are this appearance or **** by the same reference number.

[0015] As long as there is no special publication, all the structures, layers, etc. can be formed by the known conventional method with the conventional technology, or can be performed. In order to make it not restrict a nucleation limit reaction (nucleation-limiting reaction), not a nucleation limit type but diffusion control type (Nickel nickel) system salicide process is proposed. However, nickel system salicide process has the fault that thermal stability is inferior at an after [a semiconductor] process, and formation of nickel silicide tends to be influenced by the natural oxide of existence.

[0016] The Salicide method forms the silicide layer / material which carried out self-adjustment. In order to cancel these restrictions, the titanium covering nickel platinum-alloy (nickel which carried out Ti covering (Pt)) salicide process which Ti from Ti enveloping layer (protective layer) on a salicide process with the new artificer concerned, i.e., nickel of the lower part, (Pt) makes dissociate arbitrary natural oxides (SiO2), and acts as a gettering agent which permits formation of NiSi (nickel silicide) was developed.

[0017] If it explains briefly, this invention will be accompanied by the pure process which makes pure the active region and the poly gate field of a semiconductor device, in order to remove all the oxides formed on it. nickel (Pt) alloy layer is formed on the active region which it defecated, and the poly gate field. Next, Ti enveloping layer (protective layer) is formed on nickel(Pt) layer. A short-time annealing (RTA) step (process) single for nickel(Pt) silicide phase relocation in nickel(Pt) film which carried out Ti covering is adopted. Next, Salicide etchback is performed in order to remove excessive nickel (Pt) and unreacted Ti. Then, a contact process and the usual back process are performed.

[0018] Therefore, the semiconductor substrate 10 forms the poly gate 12 in the poly gate field 14 so that it may illustrate to drawing 1 . As for a semiconductor 10, being formed with silicon is desirable.

[0019] As the side-attachment-wall spacer 16 adjoins the side-attachment-wall spacer 16 and the source / drain field 18 is in an active region 20, it can adjoin and form it in the poly gate 12. The field oxide-film (FOX) field 26 can adjoin an active region 20, and can be formed in the outside of this active region 20, and this field 26 carries out the work which isolates an active region 20 from other adjoining devices or fields.

[0020] The other start structures can be used to the method of this invention. It passes over the structure illustrated to drawing 1 only to the thing for explanation.

An oxide layer 22 can be formed for a pre-Salicide pure process structure object on ****, and the source / drain and the poly gate 12 at atmosphere oxygen and/or moisture. Generally the thickness of an oxide layer 22 is about 5A or 30A.

[0021] In order to remove the oxide layer 22 which will be formed on the exposed silicon, the pre-Salicide pure process 24 is performed. For example, in order to remove the arbitrary oxides 22 from an active region 20 and the poly gate field 14, HF solution (HF:H2O is about 1:100 rate) diluted to the structure of drawing 1 is made to act for about 100 seconds or 800 seconds (it dips in HF solution which diluted the structure).

[0022] A pre-Salicide pure process removes a considerable quantity of the oxide layer

22. However, that oxide may remain a little on the source / drain field 18, or the poly gate 12 after pre-Salicide clarification. Moreover, it originates in the oxygen or the moisture in the atmosphere of the surroundings which enclose the structure before nickel(Pt) deposition step, and an additional oxide (for example, natural oxide) may be formed on the silicon exposed in the active region 20 and the poly gate field 14.
The nickel (Pt) layer 28 is made to deposit on an activity device like the structure, the poly gate 12, and the source/drain 18 (oxides arbitrary again (not shown)) so that it may illustrate to deposition drawing 2 of nickel (Pt). As for the nickel (Pt) layer 28, it is desirable to make it deposit by sputtering using (Nickel nickel) alloy metal target material containing the platinum (Pt) of about 0.2 atom % or 10 atom %. As for the thickness of the nickel (Pt) layer 28, it is desirable that they are about 50A or 300A. this deposition -- a room temperature -- or it can carry out above a room temperature Let sputtering be high-frequency (rf) sputtering or non-RF (non-rf) sputtering. Let sputtering atmosphere be the mixture of an argon or an argon, and nitrogen. Possible alloy metal target material contains nickel (Pd).
The Ti enveloping layer (protective layer) 30 is made to deposit on the nickel (Pt) layer 28 so that it may illustrate to deposition drawing 3 of Ti. It is desirable to make it deposit by sputtering, and as for the Ti enveloping layer 30, it is desirable that thickness considers as about 10A or 300A, and it is more desirable to consider as about 30A or 200A. In order to form the nickel (Pt) film 40 which carried out Ti covering, the Ti enveloping layer 30 is formed before an annealing (annealing) process. Sputtering conditions can be made into an abbreviation room temperature or 400 degrees C, without /Receiving in response to the assistance of plasma under N2, or N2 / Ar state. TiN can also be used as an enveloping layer (protective layer) 30.
After forming the Ti enveloping layer 30 so that it may illustrate to single RTA drawing 4 for NiSi formation, short-time annealing (RTA) 32 is performed to the structure for nickel(Pt) silicide phase move within the Ti covering-nickel (Pt) film 40. Layer thickness [annealing (annealing) conditions and having deposited] determines the amount of the amount of the silicide 50 and 60 formed therefore the Ti enveloping layer 30 consumed, and the nickel (Pt) layer 28. In order to form the silicide layers 50 and 60, the state of consuming a part of Ti covering 30 and nickel (Pt) layer 28 is shown in drawing 4 .
[0023] As for RTA32, it is desirable for about 10 seconds or 60 seconds to be carried out at the temperature of about 400 degrees C or 800 degrees C. The temperature rise inclination of RTA is carried out a second in about 20 degrees C /or 100 degrees C/second, and the soaking time (soak time) of RTA may be about 5 seconds or 60 seconds.
[0024] In pure nickel-Salicide formation, the nickel (Pt) layer 28 is stable at about 800 degrees C higher enough than the highest RTA temperature of about 600 degrees C. It is that the titanium from the Ti enveloping layer 30 functions as an important point of this invention while carrying out RTA32 as a gettering agent which makes arbitrary natural oxides (SiO2) dissociate between the nickel (Pt) layer 28 and the 20/poly gate field 14 of active regions. This natural oxide can be formed between a pre-Salicide pure process and the process which forms the nickel (Pt) layer 28 of drawing 2 , as it exists on the source / drain field 18, or the poly gate 12 after the pre-Salicide pure step of drawing 1 or being mentioned above. Thickness can make this natural oxide the range about 5A, 80A, or whose thickness is about 5A or 20A.
[0025] A reaction scheme (reaction scheme) is different according to the thickness of the both sides of the Ti enveloping layer 30 and the nickel (Pt) alloy layer 28, and the ratio of the relative thickness. Furthermore, since the supply heating value at the time of nickel(Pt) Salicide formation of the range of 400 degrees C or 800 degrees C is size, reaction process and the final structure are dependent also on the Salicide formation

temperature again.
The deposition Ti enveloping layer 30 of Ti and nickel (Pt) can prevent oxidization of the nickel (Pt) alloy layer 28 by forming TiO and a TiON protective layer (not shown) in the front face between annealing (annealing) 32 (RTA in N2, or N2 / Ar atmosphere).
If it is in the RTA process nickel, i.e., this case, nickel (Pt) P. As indicated by the paper "the nickel-Si phase transference time the natural oxide owner ** case / in case there is nothing" of being based on S. Lee and others Since SiO2 or a natural oxide cannot be returned, Ti from the Ti enveloping layer 30 It is spread through the nickel (Pt) alloy layer 28, and accumulates to the interface between the nickel (Pt) layer 28 and a lower layer, an oxide is returned, and [nickel(Pt)] xTiyO interlayer (not shown) is offered.
[0026] nickel (Pt) is diffused through [nickel(Pt)] xTiyO interlayer, reacts with Si, and forms the NiPtSi silicide layers 50 and 60. Unreacted nickel (Pt) remains in the crowning of a nickel(Pt) Si layer. While carrying out an etchback process with Ti system oxide (TiO) or a nitriding oxide (TiON), etching removal of these unreacted nickel (Pt) can be carried out.
[0027] The silicide layer 50 is formed on the source / drain field 18 within an active region 20, and the silicide layer 60 is formed on the poly gate 12 in the poly gate field. About 50% or 100% of nickel (Pt) layer 28 is changed into the silicide layers 50 and 60, and about 2% or 80% of Ti enveloping layer 30 (it is dependent on the thickness) returns a natural oxide.
[0028] In the case of temperature <=800 degree C, the silicide layers 50 and 60 consist of 100% of nickel(Pt) Si, and, in the case of 800 degrees C, the silicide layers 50 and 60 also contain temperature >nickel(Pt) Si2 of the amount applied to nickel(Pt) Si again.
In order to remove surplus nickel (Pt) and unreacted Ti so that it may illustrate to Salicide etchback drawing 5 , Salicide etchback is performed in the structure of drawing 4 . The mixture (H2SO4, H2O2, H2O) of a sulfur peroxide is made to act for about 1 minute or 10 minutes to the structure preferably (the structure is soaked in the mixture of a sulfur peroxide for about 1 minute or 10 minutes). As for the Salicide etchback solution of the mixture of a sulfur peroxide, it is desirable to consist of about 5% or 55% of H2SO4, about 1%, or 22.5% of H2O2 and about 1%, or 22.5% of H2O. etchback temperature -- about 30 degrees C or 80 degrees C -- it is -- about 1 minute -- or it is carried out for 30 minutes
[0029] This Salicide etchback makes the silicide layer 60 in the poly gate field 14, and the silicide layer 50 in an active region 20 expose for the further processing. Next, a contact process and the usual back process can be performed.
The advantage of the method of the advantage this invention of this invention includes the following point.
[0030] i) A natural oxide is made to dissociate while forming nickel(Pt) Si 50 and 60.;
ii) -- formation of NiSi2 is delayed and it has the more excellent condensation resistance -- thermal -- a stable nickel(Pt) Si process and a stable bird clapper, and;
The iiiTi enveloping layer 30 should prevent the oxygen contamination from circumference atmosphere.
[0031] Although the form of especially desirable operation of this invention was illustrated and explained, this does not mean limiting this invention except for the case where it is indicated by the claim.

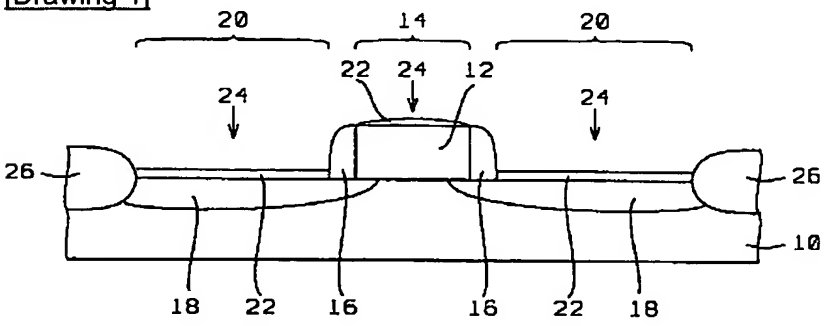
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the schematic diagram of the gestalt of desirable operation of this

invention.
[Drawing 2] It is the schematic diagram different from drawing 1 showing the gestalt of desirable operation of this invention.
[Drawing 3] It is the schematic diagram different from drawing 1 showing the gestalt of desirable operation of this invention.
[Drawing 4] It is the schematic diagram different from drawing 1 showing the gestalt of desirable operation of this invention.
[Drawing 5] It is the schematic diagram different from drawing 1 showing the gestalt of desirable operation of this invention.
[Description of Notations]
10 Semiconductor Substrate 12 Multigate
14 Multigate Field 16 Side-Attachment-Wall Spacer
18 Source / Drain Field 20 Active Region
22 Oxide Layer 24 PURESA LISA Id Pure Process
26 Field Oxidizing-Zone (FOX) Field
28 Nickel (Pt) Layer 30 Ti Enveloping Layer
32 Short-time Annealing (RTA) Process
40 Nickel (Pt) Film Which Carried Out Ti Covering
50 60 Silicide / nickel(Pt) Si

DRAWINGS

[Drawing 1]



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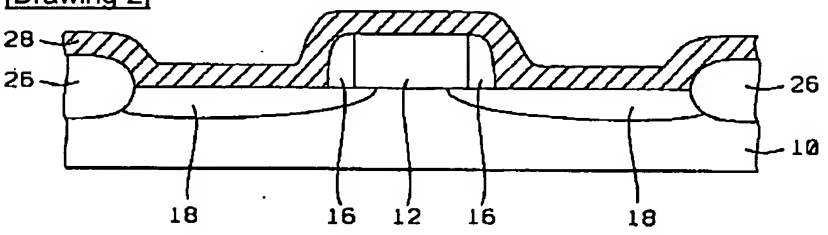

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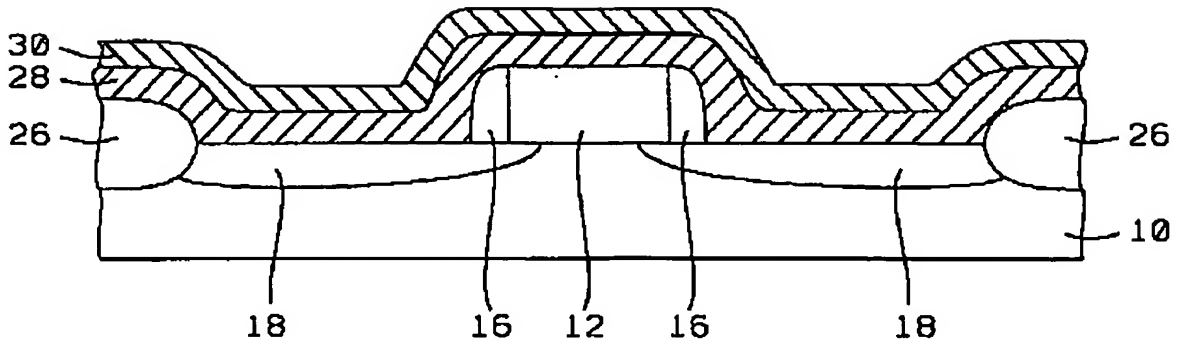

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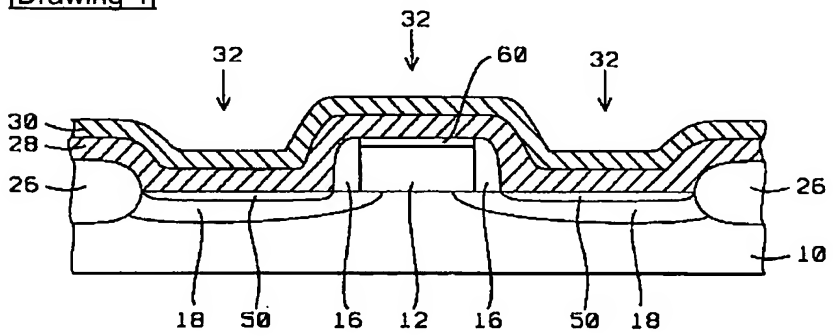

[Drawing 5]